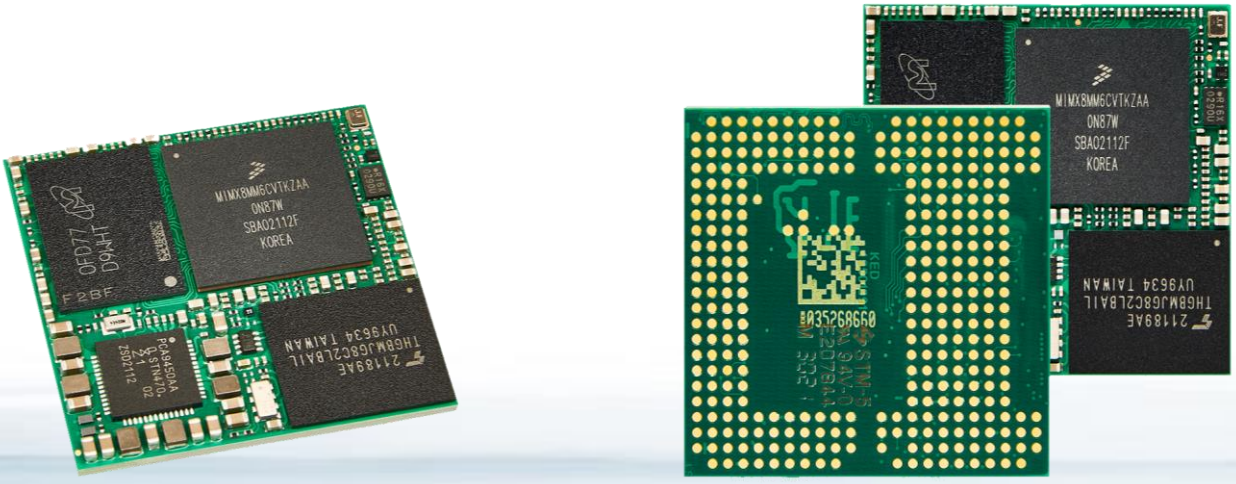
USER GUIDE



OSM-S i.MX8M Mini

Doc. Rev. 0.4

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OSM-S I.MX8M MINI - USER GUIDE

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Revision History

Revision	Brief Description of Changes	Date of Issue	Author/Editor
0.1	Basic draft	2021-04-21	Gb
0.2	Updated pin mux table	2022-01-14	Ar
0.3	Updated product name	2022-03-08	Gb
0.4	Change to OSM V1.1	2022-04-27	Gb

Customer Support

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Customer Comments

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Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements.
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1/ Introduction

This user guide describes the 30mmx30mm SoM form factor module - OSM-S i.MX8M Mini . The Advanced RISC Machines (ARM) based module is equipped with NXP i.MX8M Mini processor. The quad core SoC takes advantage of the optimized power consumption and performance ratio.

The use of this user guide implies a basic knowledge of PC hardware and software. This user guide is focused on describing the special features and is not intended to be a standard PC textbook. New users are recommended to study the short installation procedure, before switching on the power.

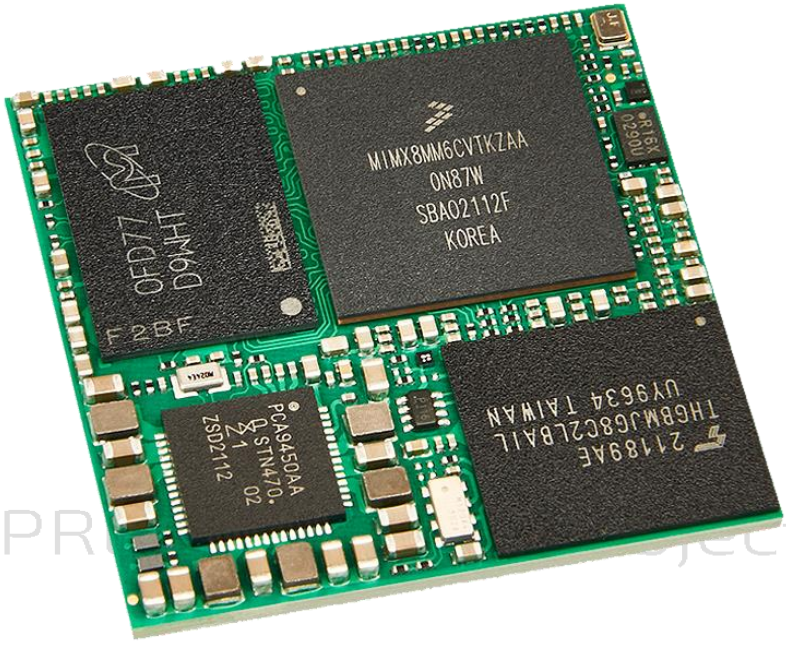
All configuration and setup of the module is performed using the u-Boot CLI.

Latest revision of this user guide, datasheet, and BSPs (Board Support Packages) can be downloaded from Kontron Electronics Web Page.

2/ Description

The OSM-S i.MX8M Mini is a very small System-on-Module (SoM) using NXPs i.MX8M Mini processor with ARM Quad Cortex A53 and Cortex M4. The OSM-S i.MX8M Mini is a highly integrated, small sized module for integration in embedded systems with 30mmx30mm footprint. The module is compatible with SGETs OSM standard sizes.
The complexity of the DDR4 memory, power management and processor connection are contained in the SOM and simplifies baseboard development.

Figure 1: 30x30mm SoM with LGA package



Main characteristics of the OSM-S i.MX8M Mini are:

- quad Arm® Cortex®-A53 core with up to 1.6 GHz and Cortex®-M4 400 MHz core processor is for low-power processing
- Up to 4 GB LPDDR4 memory down
- 4 to 64 GB eMMC
- 2 MB QSPI boot flash
- 8kB EEPROM
- 1x ultra low power RTC
- 2D GPU and 3D GPU (1x shader, OpenGL ES 2.0)
- 1x MIPI DSI (4-lane) with PHY
- 1x MIPI CSI (4-lane) with PHY
- Video Playback with 1080p60
- 2x USB 2.0 OTG controllers with integrated PHY
- 1x Gigabit Ethernet (MAC) with AVB and IEEE 1588, Energy Efficient Ethernet (EEE) for low power
- 1x PCIe 2.0 (1-lane) with L1 low power substates
- 1x I2S
- 2x SDIO
- 4x UART
- 3x I2C
- 2x SPI
- 3x PWM
- 24x GPIO

2.1. Product Variants and Accessories

Order Information:

Table 1: Product Variants of OSM-S i.MX8M Mini

Board	Description	Product Number
OSM-S i.MX8M Mini 1GB/8GB -25..+85°	SoM with NXP I.MX8M Mini quad core processor, 1 GB LPDDR4 and 8 GB eMMC	40099 227
OSM-S i.MX8M Mini 2GB/8GB -25..+85°	SoM with NXP I.MX8M Mini quad core processor, 2 GB LPDDR4 and 8 GB eMMC	40099 229
OSM-S i.MX8M Mini 4GB/32GB -25..+85°	SoM with NXP I.MX8M Mini quad core processor, 4 GB LPDDR4 and 32 GB eMMC	40099 231

Table 2: Development Kits of OSM-S i.MX8M Mini

Board	Description	Product Number

3/ System Specifications

3.1. Component Main Data

The table below summarizes the features of the SoM.

Table 2: Component Main Data

OSM-S I.MX8MM	
Form factor	30x30mm with 332 LGA pads
Processor	NXP's MIMX8MM6CVTKZAA with 14mm x 14mm BGA package in 0.5mm pitch (industrial version) up to 1.6 GHz
Memory	1.6 GHz 32-bit LPDDR4 ▶ 1 GByte: 1x 8 Gbit density 256 M x32 LPDDR4 parts ▶ 2 GByte: 1x 16 Gbit density 512 M x32 LPDDR4 parts ▶ 4 GByte: 1x 32 Gbit density 1024 M x32 LPDDR4 parts
Boot Flash	2 MB SPI NOR flash in USON (2x3mm) package connected on ECSPI1
EEPROM	8kB EEPROM on I2C1
Bootloader/BIOS	U-Boot Bootloader
embedded Multi-media Card (eMMC)	4 to 64 GB MLC (Multi-level Cell) connected on SD1
Display	▶ 1x MIPI DSI (4-lane) with PHY ▶ Resolution: up to Full-HD 1080p @60 fps
Onboard Controllers	
Ethernet Controller	▶ Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588, no phy on SoM
Watchdog Timer	CPU internal watchdog, configurable timeout counter with timeout periods from 0.5 to 128 seconds
System Management Controller	No dedicated System Management Controller on module System settings can be arranged in U-Boot environment variables
H/W Status Monitor	CPU internal temperature monitoring sensor
Power management	PCA9450AHN from NXP
RTC	1x RV-3028-C7 on I2C1, 45 nA @ 3 V, factory calibrated to ±1 ppm @ 25°C
Operating System Support	Linux Yocto
Default Interfaces	
I2C	3x (2x general purpose, 1x dedicated for PCIe and CSI)
LAN, USB	1x Gigabit Ethernet, 2x USB 2.0 OTG
Display	1x MIPI DSI (4-lane) with up to 1920 x 1080 @60fps
Camera	1x MIPI CSI (4-lane)
SD-Card	2x SDIO (1x 4bit, 1x 8bit)
UART	4x (1x console, 3x general purpose)
GPIO	24x

PWM	3x
other Connectivity	▶ 1x SAI (I2S) ▶ 2x SPI ▶ 1x PCIe
Power	
Consumption	Maximum Power consumption of the board is measured to <3,5 W
Input Voltage	Single Supply 5V ±5%

3.2. Environmental Conditions

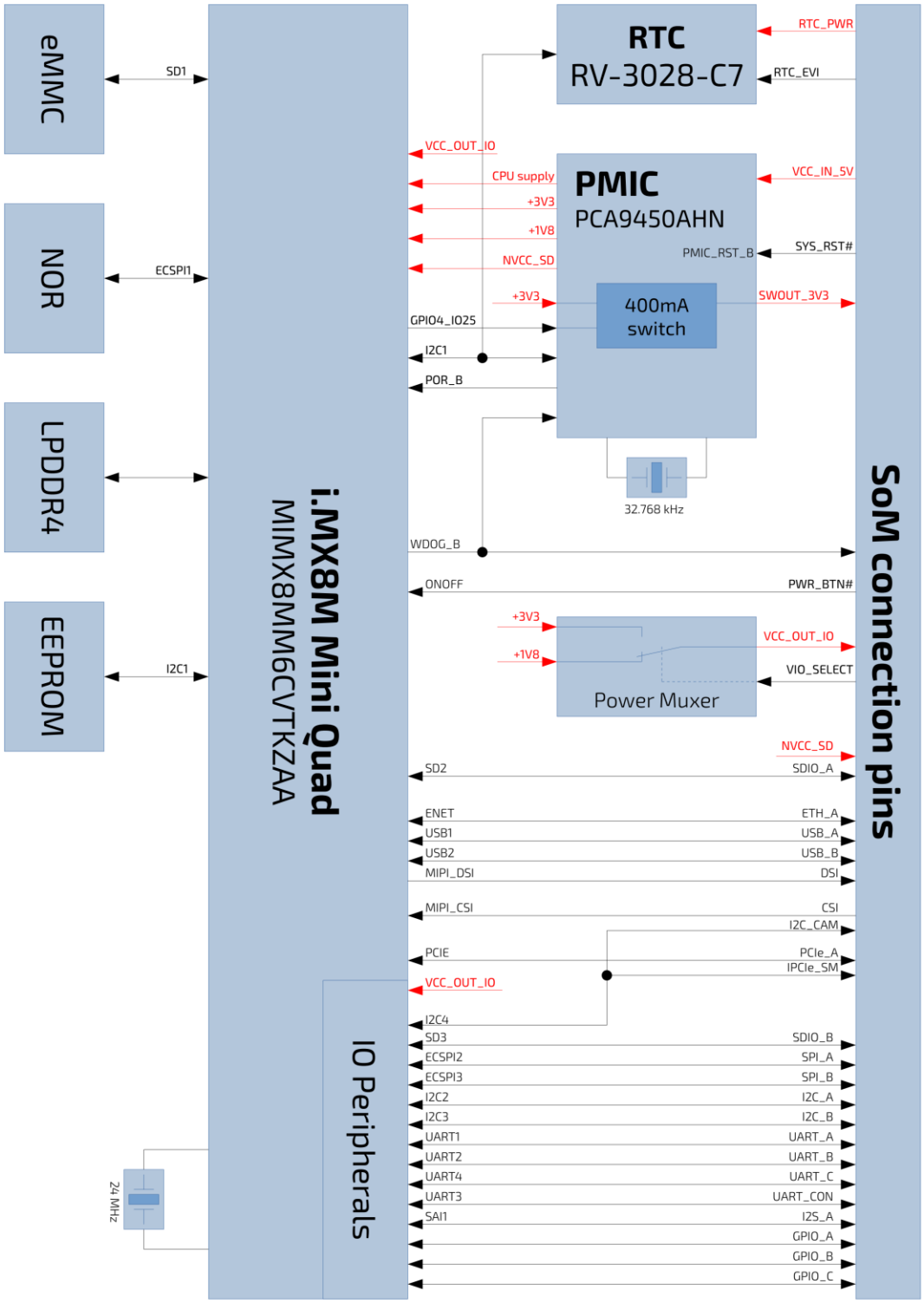
Table 3: Environmental Conditions

Operating	▶ industrial: -25°C to 85°C ▶ relative humidity (non-condensing) 10 % to 93 % at 40°C
Storage	▶ commercial grade: -40°C to +85°C ▶ relative humidity (non-condensing) 10 % to 93 % at 40°C

3.3. Functional Block Diagram

The block diagram shows a detailed structure of the OSM-S i.MX8M Mini module.

Figure 2: Block Diagram



4/ Board and Connectors

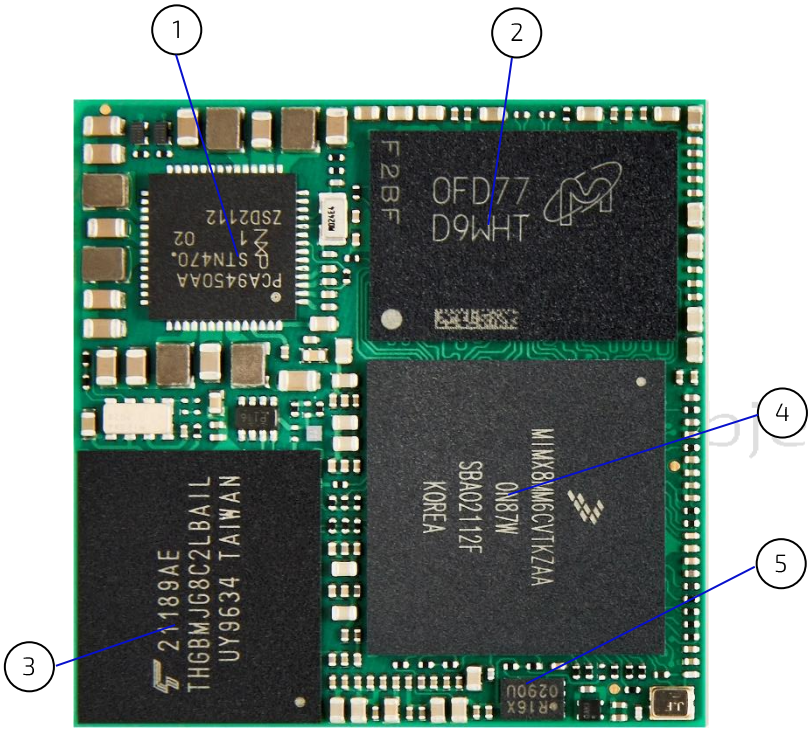
4.1.1. Connectors

Table 4: Connectors of OSM-S i.MX8M Mini

Connector	Function	Remark
LGA package	Central Interface	solderable

4.2. SoM view and locations

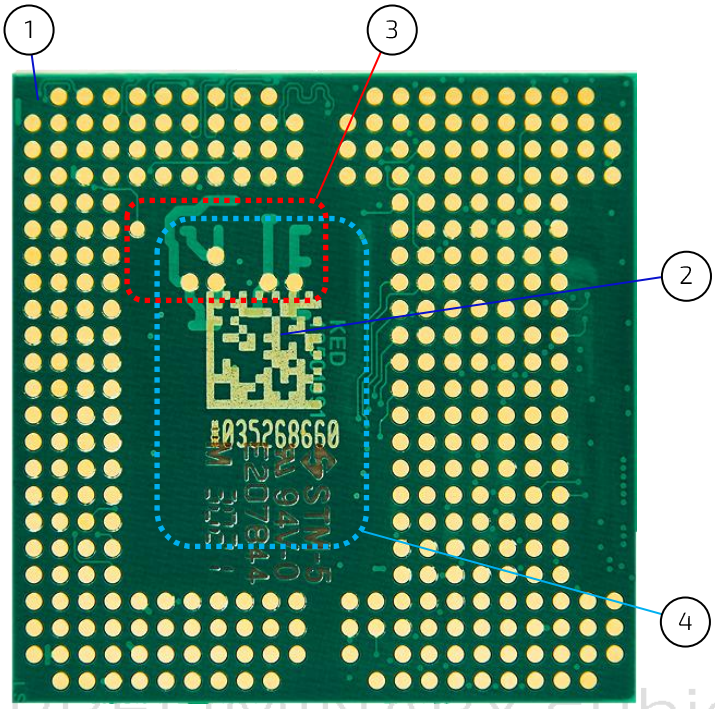
Figure 3: Top View



1. PMIC
2. LPDDR4
3. eMMC
4. i.MX8M Mini
5. NOR-Flash

4.3. Bottom Side

Figure 4: Bottom View



1. Pin 1 marking (missing pin)
2. Unique ID
3. Test points (factory use only)
4. Keep out area on base board

4.4. Mechanical Drawings

Figure 5: Dimensions of OSM-S i.MX8M Mini (top view)

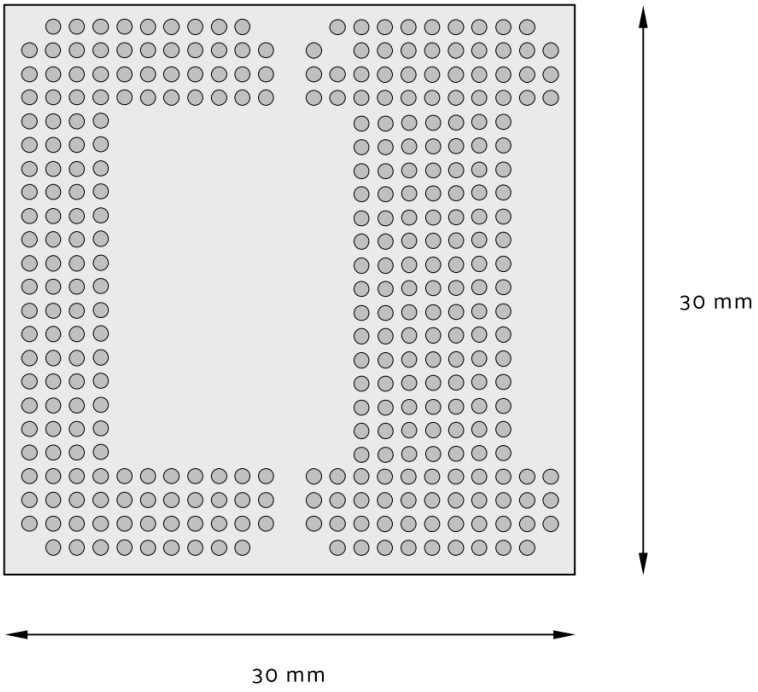


Figure 6: Footprint Grid

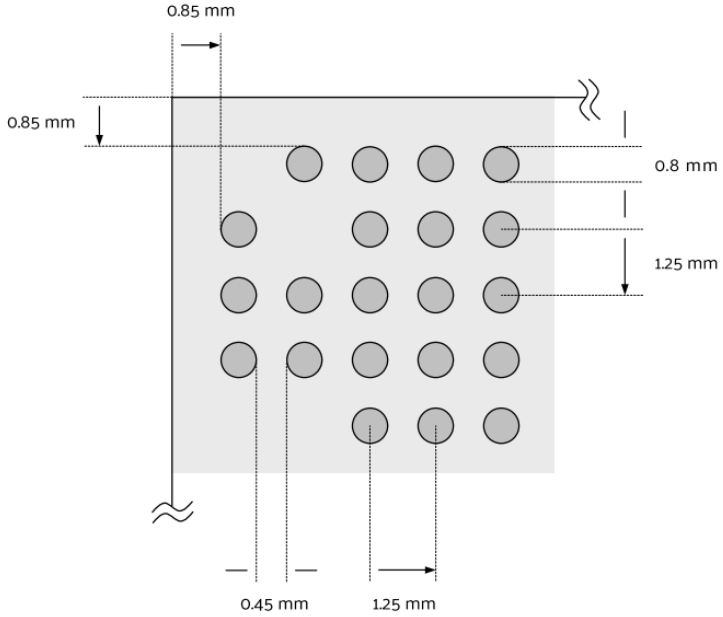
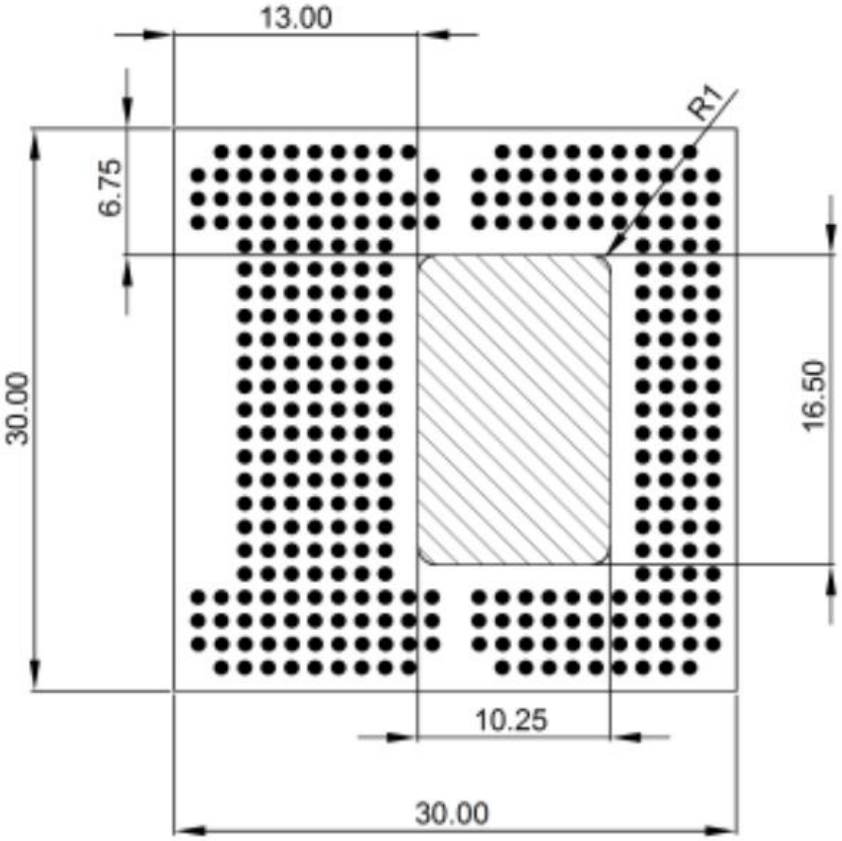
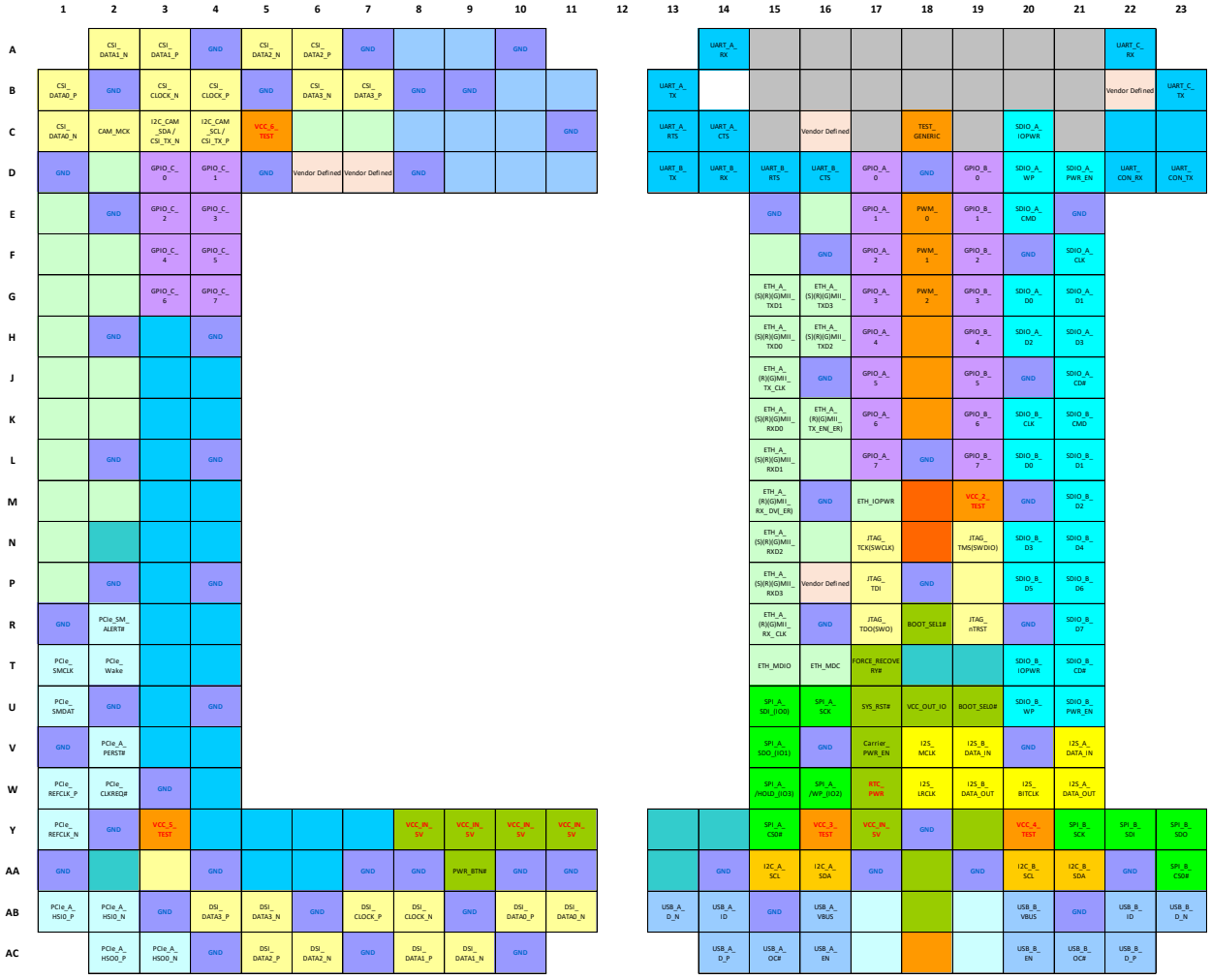


Figure 7: Keep out area on baseboard (bottom view)



4.5. Pinout diagram of OSM-S i.MX8M Mini

Figure 8: pin assignment (top view)



4.5.1. Pinout of OSM-S i.MX8M Mini

The pinout described here is the default pinout of the SoM in comparison to the OSM pinout. One can use "*Pins Tool for i.MX Application Processors*" to change the multiplexing. The tool can be downloaded from nxp homepage.

NOTICE

Changing the multiplexing creates the need of changing the device tree too.

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
VCC_2_TEST	M19	-	+0V9_VDD_DRAM&PU	Module power voltage testpoint	P	-	-	-
VCC_3_TEST	Y16	-	+0V9_VDD_ARM	Module power voltage testpoint	P	-	-	-
VCC_4_TEST	Y20	-	+0V8_VDD_SOC	Module power voltage testpoint	P	-	-	-
VCC_IN_5V	Y17	-	+5V	Module power input voltage of 5V – Primary voltage rail for size S, M and L modules	P	-	-	-
VCC_IN_3V3	Y19	-	n.c.	-	-	-	-	-
V_BAT	AA18, AB18	-	n.c.	-	-	-	-	-
GND	D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21	-	GND	Module Signal and power return and GND reference	P	-	-	-
SYS_RST#	U17	-	PMIC_RST_B	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	1.8V	PU 10K	-
CARRIER_PWR_EN	V17	SAI5_RXFS	GPIO3_IO16	Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN signal	O CMOS	V_OUT_IO	-	-
VCC_OUT_IO	U18	-	VCC_OUT_IO	Can provide IO voltage level for several interfaces to connect	P	1.8V/3.3V	-	In OSM spec, this pin is only applicable in size 0 and n.c. for all other sizes.
RTC_PWR	W17	-	RTC_PWR	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	P	-	-	-
BOOT_SEL0#	U19	SAI1_RXD3	GPIO4_IO05		I OD CMOS	V_OUT_IO	PU 10k	The boot medium is the choice of the module vendor.

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
BOOT_SEL1#	R18	SAI1_RXD4	GPIO4_IO06		I OD CMOS	V_OUT_IO	PU 10k	The boot medium is the choice of the module vendor.
FORCE_RECOVERY#	T17	BOOT_MODE0	__BOOT_MODE0	If low on carrier board module enters recovery mode.	I OD CMOS	V_OUT_IO	PU 10k	The recovery mode should be specified by module vendor.
JTAG_TCK(SWCLK)	N17	JTAG_TCK	JTAG_TCK	Test Clock	I CMOS	V_OUT_IO	-	-
JTAG_TMS(SWDIO)	N19	JTAG_TMS	JTAG_TMS	Test Mode Select	I CMOS	V_OUT_IO	-	-
JTAG_TDI	P17	JTAG_TDI	JTAG_TDI	Test Data Input	I CMOS	V_OUT_IO	-	-
JTAG_RTCK	P19	-	n.c.	-	-	-	-	-
JTAG_TDO(SWO)	R17	JTAG_TDO	JTAG_TDO	Test Data Output	O CMOS	V_OUT_IO	-	-
JTAG_nTRST	R19	JTAG_TRST_B	JTAG_TRST_B	Test Reset, Active Low	I CMOS	V_OUT_IO	-	-
DEBUG_EN	AC18		n.c.	-	-	-	-	-
TEST_GENERIC	C18	JTAG_MOD	JTAG_MOD	General purpose for testing	I CMOS	V_OUT_IO	-	high: enables boundary scan float: normal operation
UART_A_RX	A14	SAI2_RXC	UART1_RXD	Asynchronous serial data input port A	I CMOS	V_OUT_IO	-	-
UART_A_TX	B13	SAI2_RXFS	UART1_TXD	Asynchronous serial data output port A	O CMOS	V_OUT_IO	-	-
UART_A_RTS	C13	SAI2_TXFS	UART1_CTS	"Request to Send" handshake line for port A	O CMOS	V_OUT_IO	-	-
UART_A_CTS	C14	SAI2_RXD0	UART1_RTS	"Clear to Send" handshake line for port A	I CMOS	V_OUT_IO	-	-
UART_B_RX	D14	SAI3_TXFS	UART2_RXD	Asynchronous serial data input port B	I CMOS	V_OUT_IO	-	-
UART_B_TX	D13	SAI3_TXC	UART2_TXD	Asynchronous serial data output port B	O CMOS	V_OUT_IO	-	-
UART_B_RTS	D15	SAI3_RXC	UART2_CTS	"Request to Send" handshake line for port B	O CMOS	V_OUT_IO	-	-
UART_B_CTS	D16	SAI3_RXD	UART2_RTS	"Clear to Send" handshake line for port B	I CMOS	V_OUT_IO	-	-
UART_C_RX	A22	UART4_RXD	UART4_RXD	Asynchronous serial data input port C	I CMOS	V_OUT_IO	-	-
UART_C_TX	B23	UART4_TXD	UART4_TXD	Asynchronous serial data output port C	O CMOS	V_OUT_IO	-	-
UART_D_RX	C22	-	n.c.	-	-	-	-	-
UART_D_TX	C23	-	n.c.	-	-	-	-	-
UART_CON_RX	D22	UART3_RXD	UART3_RXD	Asynchronous serial data input port console	I CMOS	V_OUT_IO	-	-
UART_CON_TX	D23	UART3_TXD	UART3_TXD	Asynchronous serial data output port console	O CMOS	V_OUT_IO	-	-
ETH_A_(R)(G)MII_CRS	E16	-	n.c.	-	-	-	-	-
ETH_A_(R)(G)MII_COL	F15	-	n.c.	-	-	-	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
ETH_A_(S)(R)(G)MII_TXD0	H15	ENET_TD0	ENET_TD0	Transmit data bit 0 (transmitted first) port A	O CMOS	1.8V	-	-
ETH_A_(S)(R)(G)MII_TXD1	G15	ENET_TD1	ENET_TD1	Transmit data bit 1 port A	O CMOS	1.8V	-	-
ETH_A_(S)(R)(G)MII_TXD2	H16	ENET_TD2	ENET_TD2	Transmit data bit 2 port A	O CMOS	1.8V	-	-
ETH_A_(S)(R)(G)MII_TXD3	G16	ENET_TD3	ENET_TD3	Transmit data bit 3 port A	O CMOS	1.8V	-	-
ETH_A_(R)(G)MII_TX_EN(_ER)	K16	ENET_TX_CTL	ENET_TX_CTL	Transmit enable (Error) port A	O CMOS	1.8V	-	-
ETH_A_(R)(G)MII_TX_CLK	J15	ENET_TXC	ENET_TXC	Transmit clock port A	I/O CMOS	1.8V	-	-
ETH_A_(S)(R)(G)MII_RXD0	K15	ENET_RD0	ENET_RD0	Receive data bit 0 (received first) port A	I CMOS	1.8V	-	-
ETH_A_(S)(R)(G)MII_RXD1	L15	ENET_RD1	ENET_RD1	Receive data bit 1 port A	I CMOS	1.8V	-	-
ETH_A_(R)(G)MII_RXD2	N15	ENET_RD2	ENET_RD2	Receive data bit 2 port A	I CMOS	1.8V	-	-
ETH_A_(R)(G)MII_RXD3	P15	ENET_RD3	ENET_RD3	Receive data bit 3 port A	I CMOS	1.8V	-	-
ETH_A_(R)(G)MII_RX_ER	L16	-	n.c.	-	-	-	-	-
ETH_A_(R)(G)MII_RX_DV(_ER)	M15	ENET_RX_CTL	ENET_RX_CTL	Receive data valid port A	I CMOS	1.8V	-	-
ETH_A_(R)(G)MII_RX_CLK	R15	ENET_RXC	ENET_RXC	Receive clock port A	I/O CMOS	1.8V	-	-
ETH_A_SDP	N16	-	n.c.	-	-	-	-	-
ETH_MDIO	T15	ENET_MDIO	ENET_MDIO_1V8	Management data	I/O CMOS	1.8V	-	-
ETH_MDC	T16	ENET_MDC	ENET_MDC_1V8	Management data clock	O CMOS	1.8V	-	-
ETH_IOPWR	M17	-	+1V8	ETH voltage. It is used to provide the IO Voltage Level for all Ethernet interfaces.	P	1.8V		Minimum current: 100mA
GPIO_A_0	D17	GPIO1_IO01	GPIO1_IO01	General purpose I/O Contact A0	I/O CMOS	V_OUT_IO	-	-
GPIO_A_1	E17	GPIO1_IO03	GPIO1_IO03	General purpose I/O Contact A1	I/O CMOS	V_OUT_IO	-	-
GPIO_A_2	F17	GPIO1_IO05	GPIO1_IO05	General purpose I/O Contact A2	I/O CMOS	V_OUT_IO	-	-
GPIO_A_3	G17	GPIO1_IO06	GPIO1_IO06	General purpose I/O Contact A3	I/O CMOS	V_OUT_IO	-	-
GPIO_A_4	H17	GPIO1_IO07	GPIO1_IO07	General purpose I/O Contact A4	I/O CMOS	V_OUT_IO	-	-
GPIO_A_5	J17	GPIO1_IO08	GPIO1_IO08	General purpose I/O Contact A5	I/O CMOS	V_OUT_IO	-	-
GPIO_A_6	K17	GPIO1_IO09	GPIO1_IO09	General purpose I/O Contact A6	I/O CMOS	V_OUT_IO	-	-
GPIO_A_7	L17	GPIO1_IO10	GPIO1_IO10	General purpose I/O Contact A7	I/O CMOS	V_OUT_IO	-	-
GPIO_B_0	D19	GPIO1_IO11	GPIO1_IO11	General purpose I/O Contact B0	I/O CMOS	V_OUT_IO	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
GPIO_B_1	E19	GPIO1_IO12	GPIO1_IO12	General purpose I/O Contact B1	I/O CMOS	V_OUT_IO	-	-
GPIO_B_2	F19	SAI5_RXFS	GPIO3_IO19	General purpose I/O Contact B2	I/O CMOS	V_OUT_IO	-	-
GPIO_B_3	G19	SAI5_RXC	GPIO3_IO21	General purpose I/O Contact B3	I/O CMOS	V_OUT_IO	-	-
GPIO_B_4	H19	SAI1_RXD2	GPIO4_IO04	General purpose I/O Contact B4	I/O CMOS	V_OUT_IO	-	-
GPIO_B_5	J19	SAI1_TXD2	GPIO4_IO14	General purpose I/O Contact B5	I/O CMOS	V_OUT_IO	-	-
GPIO_B_6	K19	SAI1_TXD3	GPIO4_IO15	General purpose I/O Contact B6	I/O CMOS	V_OUT_IO	-	-
GPIO_B_7	L19	SAI1_TXD4	GPIO4_IO16	General purpose I/O Contact B7	I/O CMOS	V_OUT_IO	-	-
SDIO_A_CMD	E20	SD2_CMD	SD2_CMD	SDIO A Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_A_CLK	F21	SD2_CLK	SD2_CLK	SDIO A Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	-	-
SDIO_A_D0	G20	SD2_DATA0	SD2_DATA0	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_A_D1	G21	SD2_DATA1	SD2_DATA1	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_A_D2	H20	SD2_DATA2	SD2_DATA2	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_A_D3	H21	SD2_DATA3	SD2_DATA3	SDIO A Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_A_CD#	J21	SD2_CD_B	SD2_CD_B	SDIO A Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	1.8V or 3.3V	PU 10k	-
SDIO_A_WP	D20	SD2_WP	SD2_WP	SDIO A Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	1.8V or 3.3V	PU 10k	Tie to GND on carrier, if not used
SDIO_A_PWR_EN	D21	SD2_RESET_B	GPIO2_IO19	SDIO A Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	1.8V or 3.3V	-	-
SDIO_A_IOPWR	C20	-	NVCC_SD	SDIO A Voltage. It is used to provide the IO Voltage Level	P	1.8V or 3.3V	-	Minimum current: 100mA
SDIO_B_CLK	K20	NAND_WE_B	SD3_CLK	SDIO B Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	-	-
SDIO_B_CMD	K21	NAND_WP_B	SD3_CMD	SDIO B Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_D0	L20	NAND_DATA04	SD3_DATA0	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_D1	L21	NAND_DATA05	SD3_DATA1	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
SDIO_B_D2	M21	NAND_DATA06	SD3_DATA2	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_D3	N20	NAND_DATA07	SD3_DATA3	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_D4	N21	NAND_RE_B	SD3_DATA4	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_D5	P20	NAND_CE2_B	SD3_DATA5	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_D6	P21	NAND_CE3_B	SD3_DATA6	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_D7	R21	NAND_CLE	SD3_DATA7	SDIO B Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	-	-
SDIO_B_CD#	T21	NAND_CE1_B	GPIO3_IO02	SDIO B Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	1.8V or 3.3V	PU 10k	-
SDIO_B_WP	U20	SAI3_MCLK	GPIO5_IO02	SDIO B Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	1.8V or 3.3V	PU 10k	Tie to GND on carrier, if not used
SDIO_B_IOPWR	T20	-	VCC_OUT_IO	SDIO B Voltage. It is used to provide the IO Voltage Level	P	1.8V or 3.3V	-	Minimum current: 100mA
SDIO_B_PWR_EN	U21	SAI3_TXD	GPIO5_IO01	SDIO B Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	1.8V or 3.3V	-	-
PWM_0	E18	SPDIF_EXT_CLK	PWM1_OUT	Pulse width modulation 0	O CMOS	V_OUT_IO	-	-
PWM_1	F18	SPDIF_RX	PWM2_OUT	Pulse width modulation 1	O CMOS	V_OUT_IO	-	-
PWM_2	G18	SPDIF_TX	PWM3_OUT	Pulse width modulation 2	O CMOS	V_OUT_IO	-	-
PWM_3	H18	-	n.c.	-	-	-	-	-
PWM_4	J18	-	n.c.	-	-	-	-	-
PWM_5	K18	-	n.c.	-	-	-	-	-
ADC_0	M18	-	n.c.	-	-	-	-	-
ADC_1	N18	-	n.c.	-	-	-	-	-
SPI_A_SDI_(IO0)	U15	ECSPI2_MISO	ECSPI2_MISO	SPI A Serial Data Input	IO CMOS	V_OUT_IO	-	-
SPI_A_SDO_(IO1)	V15	ECSPI2_MOSI	ECSPI2_MOSI	SPI A Serial Data Output	IO CMOS	V_OUT_IO	-	-
SPI_A_/WP_(IO2)	W16	SAI1_TXD5	GPIO4_IO17	SPI A Write Protect	IO CMOS	V_OUT_IO	-	-
SPI_A_/HOLD_(IO3)	W15	SAI1_TXD6	GPIO4_IO18	SPI A Suspends Serial Input	IO CMOS	V_OUT_IO	-	-
SPI_A_CS0#	Y15	ECSPI2_SS0	ECSPI2_SS0	SPI A Master Chip Select 0	O CMOS	V_OUT_IO	-	-
SPI_A_SCK	U16	ECSPI2_SCLK	ECSPI2_SCLK	SPI A Serial Data Clock	O CMOS	V_OUT_IO	-	-
SPI_B_SDI	Y22	UART2_RXD	ECSPI3_MISO	SPI B Serial Data Input	I CMOS	V_OUT_IO	-	-
SPI_B_SDO	Y23	UART1_TXD	ECSPI3_MOSI	SPI B Serial Data Output	O CMOS	V_OUT_IO	-	-
SPI_B_CS0#	AA23	UART2_TXD	ECSPI3_SS0	SPI B Master Chip Select 0	O CMOS	V_OUT_IO	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
SPI_B_SCK	Y21	UART1_RXD	ECSPI3_SCLK	SPI B Serial Data Clock	O CMOS	V_OUT_IO	-	-
I2S_A_DATA_IN	V21	SAI1_RXD0	SAI1_RXD0	I2S A Digital audio Input	I/O CMOS	V_OUT_IO	-	-
I2S_A_DATA_OUT	W21	SAI1_TXD0	SAI1_TXD0	I2S A Digital audio Output	I/O CMOS	V_OUT_IO	-	-
I2S_B_DATA_IN	V19	SAI1_RXD1	SAI1_RXD1	I2S B Digital audio Input	I/O CMOS	V_OUT_IO	-	-
I2S_B_DATA_OUT	W19	SAI1_TXD1	SAI1_TXD1	I2S B Digital audio Output	I/O CMOS	V_OUT_IO	-	-
I2S_MCLK	V18	SAI1_MCLK	SAI1_MCLK	Master clock output to I2S codec(s)	I/O CMOS	V_OUT_IO	-	-
I2S_LRCLK	W18	SAI1_TXFS	SAI1_TXFS	I2S Left & Right synchronization clock	I/O CMOS	V_OUT_IO	-	Module Output if CPU acts in Master Mode, Module Input if CPU acts in Slave Mode
I2S_BITCLK	W20	SAI1_TXC	SAI1_TXC	I2S Digital audio clock	I/O CMOS	V_OUT_IO	-	Module Output if CPU acts in Master Mode, Module Input if CPU acts in Slave Mode
CAN_A_TX	AC17	-	n.c.	-	-	-	-	-
CAN_A_RX	AB17	-	n.c.	-	-	-	-	-
CAN_B_TX	AC19	-	n.c.	-	-	-	-	-
CAN_B_RX	AB19	-	n.c.	-	-	-	-	-
USB_A_D_N	AB13	USB1_DN	USB1_DN	USB differential data pairs for port A	I/O USB	USB	-	-
USB_A_D_P	AC14	USB1_DP	USB1_DP	USB differential data pairs for port A	I/O USB	USB	-	-
USB_A_ID	AB14	USB1_ID	USB1_ID_1V8	Input Contact to announce OTG device insertion on USB 2.0 port	I CMOS	1.8V	PU 10k	-
USB_A_OC#	AC15	GPIO1_IO13	USB1_OC	USB over-current for port A	I OD CMOS	V_OUT_IO	PU 10k	-
USB_A_VBUS	AB16	USB1_VBUS	USB1_VBUS	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V	-	-
USB_A_EN	AC16	SAI5_MCLK	GPIO3_IO25	Power enable for usb VBUS voltage	O CMOS	V_OUT_IO	-	-
USB_B_D_N	AB23	USB2_DN	USB2_DN	USB differential data pairs for port B	I/O USB	USB	-	-
USB_B_D_P	AC22	USB2_DP	USB2_DP	USB differential data pairs for port B	I/O USB	USB	-	-
USB_B_ID	AB22	USB2_ID_1V8	USB2_ID_1V8	Input Contact to announce OTG device insertion on USB 2.0 port	I CMOS	1.8V	PU 10k	-
USB_B_OC#	AC21	GPIO1_IO15	USB2_OC	USB over-current for port B	I OD CMOS	V_OUT_IO	PU 10k	-
USB_B_VBUS	AB20	USB2_VBUS	USB2_VBUS	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V	-	-
USB_B_EN	AC20	SAI5_RXC	GPIO3_IO20	Power enable for usb VBUS voltage	O CMOS	V_OUT_IO	-	-
I2C_A_SCL	AA15	I2C2_SCL	I2C2_SCL	I2C Port A Clock Signal	I/O OD CMOS	V_OUT_IO	PU 2k2	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
I2C_A_SDA	AA16	I2C2_SDA	I2C2_SDA	I2C Port A Data Signal	I/O OD CMOS	V_OUT_IO	PU 2k2	-
I2C_B_SCL	AA20	I2C3_SCL	I2C3_SCL	I2C Port B Clock Signal	I/O OD CMOS	V_OUT_IO	PU 2k2	-
I2C_B_SDA	AA21	I2C3_SDA	I2C3_SDA	I2C Port B Data Signal	I/O OD CMOS	V_OUT_IO	PU 2k2	-
COM_AREA_01	A15	-	n.c.	-	-	-	-	-
COM_AREA_02	A16	-	n.c.	-	-	-	-	-
COM_AREA_03	A17	-	n.c.	-	-	-	-	-
COM_AREA_04	A18	-	n.c.	-	-	-	-	-
COM_AREA_05	A19	-	n.c.	-	-	-	-	-
COM_AREA_06	A20	-	n.c.	-	-	-	-	-
COM_AREA_07	A21	-	n.c.	-	-	-	-	-
COM_AREA_08	B15	-	n.c.	-	-	-	-	-
COM_AREA_09	B16	-	n.c.	-	-	-	-	-
COM_AREA_10	B17	-	n.c.	-	-	-	-	-
COM_AREA_11	B18	-	n.c.	-	-	-	-	-
COM_AREA_12	B19	-	n.c.	-	-	-	-	-
COM_AREA_13	B20	-	n.c.	-	-	-	-	-
COM_AREA_14	B21	-	n.c.	-	-	-	-	-
COM_AREA_15	C15	-	n.c.	-	-	-	-	-
COM_AREA_16	C17	-	n.c.	-	-	-	-	-
COM_AREA_17	C19	-	n.c.	-	-	-	-	-
COM_AREA_18	C21	-	n.c.	-	-	-	-	-
RESERVED	T18, T19, Y13, Y14, AA13	-	n.c.	Reserved for future use	-	-	-	-
Vendor Defined	B22	-	VIO_SELECT	Defined by module manufacturer	I OD CMOS	1.8V	PU 10k	float: V_OUT_IO=1.8V GND: V_OUT_IO=3.3V
Vendor Defined	C16	-	RTC_EVI	Defined by module manufacturer	I OD CMOS	RTC_PWR	PU 10k	-
Vendor Defined	P16	-	WDOG_B	Defined by module manufacturer	O CMOS	V_OUT_IO	-	-
VCC_5_TEST	Y3	-	+3V3	Module power voltage test point	P	-	-	can be used on baseboard
VCC_6_TEST	C5	-	+1V8	Module power voltage test point	P	-	-	can be used on baseboard
VCC_IN_5V	Y8, Y9, Y10, Y11	-	+5V	Module power input voltage of 5V	P	-	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
GND	A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10	-	GND	Module Signal and power return and GND reference	P	-	-	-
PWR_BTN#	AA9	ONOFF	ONOFF	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	1.8V	PU 10K	-
ETH_B_(R)(G)MII_CRS	D2	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_COL	E1	-	n.c.	-	-	-	-	-
ETH_B_(S)(R)(G)MII_TXD0	G1	-	n.c.	-	-	-	-	-
ETH_B_(S)(R)(G)MII_TXD1	F1	-	n.c.	-	-	-	-	-
ETH_B_(S)(R)(G)MII_TXD2	G2	-	n.c.	-	-	-	-	-
ETH_B_(S)(R)(G)MII_TXD3	F2	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_TX_EN(_ER)	J2	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_TX_CLK	H1	-	n.c.	-	-	-	-	-
ETH_B_(S)(R)(G)MII_RXD0	J1	-	n.c.	-	-	-	-	-
ETH_B_(S)(R)(G)MII_RXD1	K1	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_RXD2	M1	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_RXD3	N1	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_RX_ER	K2	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_RX_DV(_ER)	L1	-	n.c.	-	-	-	-	-
ETH_B_(R)(G)MII_RX_CLK	P1	-	n.c.	-	-	-	-	-
ETH_B_SDP	M2	-	n.c.	-	-	-	-	-
ETH_B_MDIO	C7	-	n.c.	-	-	-	-	-
ETH_B_MDC	C6	-	n.c.	-	-	-	-	-
GPIO_C_0	D3	NAND_DATA00	GPIO3_IO06	General purpose I/O Contact C0	I/O CMOS	V_OUT_IO	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
GPIO_C_1	D4	NAND_DATA01	GPIO3_IO07	General purpose I/O Contact C1	I/O CMOS	V_OUT_IO	-	-
GPIO_C_2	E3	NAND_DATA02	GPIO3_IO08	General purpose I/O Contact C2	I/O CMOS	V_OUT_IO	-	-
GPIO_C_3	E4	NAND_DATA03	GPIO3_IO09	General purpose I/O Contact C3	I/O CMOS	V_OUT_IO	-	-
GPIO_C_4	F3	NAND_CE0_B	GPIO3_IO01	General purpose I/O Contact C4	I/O CMOS	V_OUT_IO	-	-
GPIO_C_5	F4	NAND_ALE	GPIO3_IO00	General purpose I/O Contact C5	I/O CMOS	V_OUT_IO	-	-
GPIO_C_6	G3	SAI1_TXD7	GPIO4_IO19	General purpose I/O Contact C6	I/O CMOS	V_OUT_IO	-	Dual function: CAM_PWR
GPIO_C_7	G4	SAI1_RXFS	GPIO4_IO00	General purpose I/O Contact C7	I/O CMOS	V_OUT_IO	-	Dual function: CAM_RST#
DSI_DATA0_N	AB11	MIPI_DSI_D0_N	MIPI_DSI_D0_N	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_DATA0_P	AB10	MIPI_DSI_D0_P	MIPI_DSI_D0_P	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_DATA1_N	AC9	MIPI_DSI_D1_N	MIPI_DSI_D1_N	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_DATA1_P	AC8	MIPI_DSI_D1_P	MIPI_DSI_D1_P	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_DATA2_N	AC6	MIPI_DSI_D2_N	MIPI_DSI_D2_N	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_DATA2_P	AC5	MIPI_DSI_D2_P	MIPI_DSI_D2_P	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_DATA3_N	AB5	MIPI_DSI_D3_N	MIPI_DSI_D3_N	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_DATA3_P	AB4	MIPI_DSI_D3_P	MIPI_DSI_D3_P	DSI differential output (point to point)	O LVDS D-PHY	-	-	-
DSI_CLOCK_N	AB8	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N	DSI differential clock output (point to point)	O LVDS D-PHY	-	-	-
DSI_CLOCK_P	AB7	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P	DSI differential clock output (point to point)	O LVDS D-PHY	-	-	-
DSI_TE	AA3	-	n.c.	-	-	-	-	-
CSI_DATA0_N	C1	MIPI_CSI_D0_N	MIPI_CSI_D0_N	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_DATA0_P	B1	MIPI_CSI_D0_P	MIPI_CSI_D0_P	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_DATA1_N	A2	MIPI_CSI_D1_N	MIPI_CSI_D1_N	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_DATA1_P	A3	MIPI_CSI_D1_P	MIPI_CSI_D1_P	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_DATA2_N	A5	MIPI_CSI_D2_N	MIPI_CSI_D2_N	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_DATA2_P	A6	MIPI_CSI_D2_P	MIPI_CSI_D2_P	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_DATA3_N	B6	MIPI_CSI_D3_N	MIPI_CSI_D3_N	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_DATA3_P	B7	MIPI_CSI_D3_P	MIPI_CSI_D3_P	CSI differential input (point to point)	I LVDS D-PHY	-	-	-
CSI_CLOCK_N	B3	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N	CSI differential clock input (point to point)	I LVDS D-PHY	-	-	-
CSI_CLOCK_P	B4	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P	CSI differential clock input (point to point)	I LVDS D-PHY	-	-	-
CAM_MCK	C2	GPIO1_IO14	CCM_CLKO1	Master clock output	O CMOS	V_OUT_IO	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
I2C_CAM_SDA	C3	I2C4_SDA	I2C4_SDA	I2C data for serial camera data support link	I/O OD CMOS	V_OUT_IO	PU 2.2K	-
I2C_CAM_SCL	C4	I2C4_SCL	I2C4_SCL	I2C clock for serial camera data support link	O OD CMOS	V_OUT_IO	PU 2.2K	-
CAM_PWR / GPIO_C_6	G3	SAI1_TXD7	GPIO4_IO19	Camera 0 Power Enable, active high output.	O CMOS	V_OUT_IO	-	-
CAM_RST# / GPIO_C_7	G4	SAI1_RXFS	GPIO4_IO00	Camera 0 reset, active low output	O CMOS	V_OUT_IO	-	-
RGB_R0	Y7	-	n.c.	-	-	-	-	-
RGB_R1	AA6	-	n.c.	-	-	-	-	-
RGB_R2	Y6	-	n.c.	-	-	-	-	-
RGB_R3	AA5	-	n.c.	-	-	-	-	-
RGB_R4	Y5	-	n.c.	-	-	-	-	-
RGB_R5	Y4	-	n.c.	-	-	-	-	-
RGB_G0	W4	-	n.c.	-	-	-	-	-
RGB_G1	V3	-	n.c.	-	-	-	-	-
RGB_G2	V4	-	n.c.	-	-	-	-	-
RGB_G3	U3	-	n.c.	-	-	-	-	-
RGB_G4	T3	-	n.c.	-	-	-	-	-
RGB_G5	T4	-	n.c.	-	-	-	-	-
RGB_B0	R4	-	n.c.	-	-	-	-	-
RGB_B1	R3	-	n.c.	-	-	-	-	-
RGB_B2	P3	-	n.c.	-	-	-	-	-
RGB_B3	N3	-	n.c.	-	-	-	-	-
RGB_B4	N4	-	n.c.	-	-	-	-	-
RGB_B5	M3	-	n.c.	-	-	-	-	-
RGB_CS#	H3	-	n.c.	-	-	-	-	-
RGB_(PIXEL)CLK	M4	-	n.c.	-	-	-	-	-
RGB_HSYNC	K3	-	n.c.	-	-	-	-	-
RGB_VSYNC	L3	-	n.c.	-	-	-	-	-
RGB_DISP	K4	-	n.c.	-	-	-	-	-
RGB_DE	J4	-	n.c.	-	-	-	-	-
RGB_RESET#	J3	-	n.c.	-	-	-	-	-

Contact Name OSM	Contact Acronym	CPU Contact	Signal Name	Functional Description	I/O Type	I/O Level	PU / PD	Comments
USB_C_D_N	D11	-	n.c.	-	-	-	-	-
USB_C_D_P	D10	-	n.c.	-	-	-	-	-
USB_C_ID	D9	-	n.c.	-	-	-	-	-
USB_C_OC#	C8	-	n.c.	-	-	-	-	-
USB_C_VBUS	C9	-	n.c.	-	-	-	-	-
USB_C_EN	C10	-	n.c.	-	-	-	-	-
USB_C_SSTX_N	A9	-	n.c.	-	-	-	-	-
USB_C_SSTX_P	A8	-	n.c.	-	-	-	-	-
USB_C_SSRX_N	B11	-	n.c.	-	-	-	-	-
USB_C_SSRX_P	B10	-	n.c.	-	-	-	-	-
PCIe_A_HSI0_P	AB1	PCIE_RXN_P	PCIE_RXN_P	Differential PCIe link A receive data pair	I LVDS PCIE	-	-	AC coupled off module
PCIe_A_HSI0_N	AB2	PCIE_RXN_N	PCIE_RXN_N	Differential PCIe link A receive data pair	I LVDS PCIE	-	-	AC coupled off module
PCIe_A_HSO0_P	AC2	PCIE_TXN_P	PCIE_TXN_P	Differential PCIe link A transmit data pair	O LVDS PCIE	-	-	AC coupled off module
PCIe_A_HSO0_N	AC3	PCIE_TXN_N	PCIE_TXN_N	Differential PCIe link A transmit data pair	O LVDS PCIE	-	-	AC coupled off module
PCIe_CLKREQ#	W2	SAI5_RXD1	GPIO3_IO22	PCIe reference clock request	I OD CMOS	V_OUT_IO	PU 10k	-
PCIe_A_PERST#	V2	SAI5_RXD2	GPIO3_IO23	PCIe Port A reset output	O CMOS	V_OUT_IO	-	-
PCIe_REFCLK_P	W1	PCIE_CLK_P	PCIE_CLK_P	Differential PCIe reference clock output	O LVDS PCIE	-	-	-
PCIe_REFCLK_N	Y1	PCIE_CLK_N	PCIE_CLK_N	Differential PCIe reference clock output	O LVDS PCIE	-	-	-
PCIe_WAKE#	T2	GPIO3_IO24	GPIO3_IO24	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	I OD CMOS	V_OUT_IO	PU 10k	-
PCIe_SMDAT	U1	I2C4_SDA	I2C4_SDA	System management I2C bus DATA	I/O OD CMOS	V_OUT_IO	PU 2k2	shared with I2C_CAM_SDA
PCIe_SMCLK	T1	I2C4_SCL	I2C4_SCL	System management I2C bus CLK	O OD CMOS	V_OUT_IO	PU 2k2	shared with I2C_CAM_SCL
PCIe_SM_ALERT#	R2	GPIO4_IO28	GPIO4_IO28	SMBus Alert# (interrupt) signal	I OD CMOS	V_OUT_IO	PU 2k2	-
RESERVED	N2, AA2	-	n.c.	-	-	-	-	-
Vendor Defined	D6	CLKOUT1	CLKOUT1	-	O CMOS	1.8V	-	-
Vendor Defined	D7	CLKOUT2	CLKOUT2	-	O CMOS	1.8V	-	-

Table 5: Pinout of OSM-S i.MX8M Mini

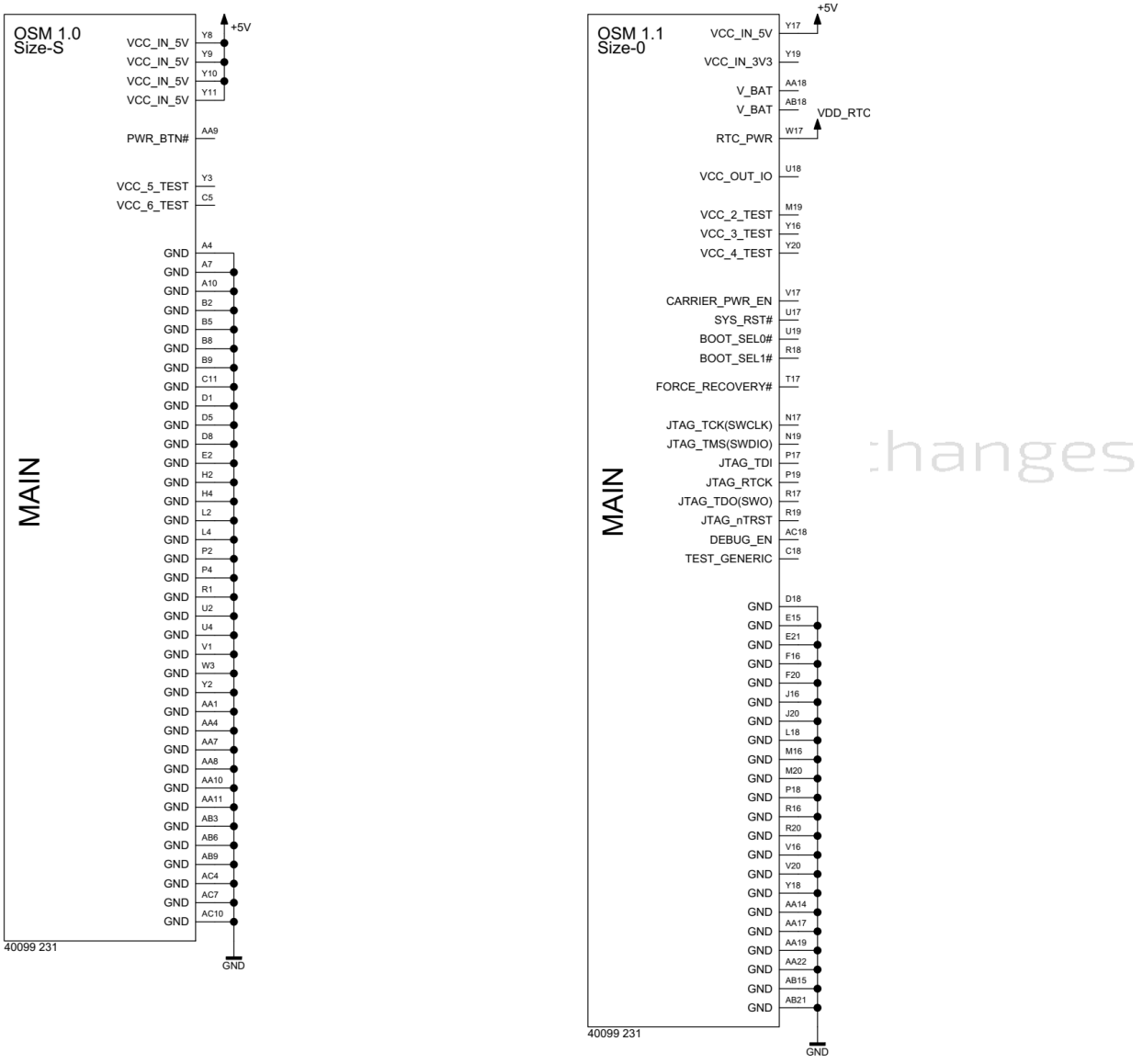
5/ Installation

5.1. Power Control

5.1.1. Power Supply

The SoM can be powered from a single 5V power source at VCC_IN_5V pins. If the RTC is used RTC_PWR also needs to be powered. OSM pins VCC_IN_3V3 and V_BAT are not used.

Figure 9: power supply scheme



The following parameters should be delivered from the carrier board:

- Voltage Ripple maximum 100 mV peak to peak 0-20 MHz to 20 ms rise time from input voltage <10% to nominal VCC

5.1.2. Supply voltage

Table 6: Supply voltage

Voltage	nominal	min	max
VCC_IN_5V	5.0	4.5	5.5
RTC_PWR	3.0	1.1	5.5

5.1.3. Supply current

The supply current is measured on the SoM using the following commands:

Stresstest on all 4 CPUs:

```
stress-ng --matrix 0 -t 0
```

Stresstest on all 4 CPUs and RAM:

```
stress-ng --matrix 0 -t 0 --vm 4 --vm-bytes 50%
```

Table 7: Supply current

Use case	mean	max peak
Linux running	TBD	TBD
stresstest on 4xCPU	TBD	TBD
stresstest on 4xCPU and RAM	TBD	TBD
stresstest on 4xCPU, RAM and GPU	TBD	TBD

5.1.4. Output Voltage

The SoM has some power output pins that can be used on the baseboard. The voltage test pins VCC_6_TEST (C5) and VCC_5_TEST (Y3) can also be used, all other VCC_X_TEST pins should not be used.

pin	nom voltage	max current
VCC_6_TEST	+3.3 V	500 mA
VCC_5_TEST	+1.8 V	500 mA
VCC_OUT_IO / SDIO_B_IOPWR	+1.8 V / +3.3 V	500 mA
NVCC_SD	+1.8 V / +3.3 V	100 mA

NOTICE

There is no current limiting device for the voltage outputs. Drawing to much current may damage the device and/or lead to malfunction.

5.1.5. IO voltage

As defined by the OSM standard, the IO voltage of the most pins is +1.8V by default (except size-0). As many systems still may run with +3.3V kontrons OSM SoM offers the possibility to switch IO voltage to +3.3V by pulling vendor defined pin B22 to GND. This voltage is also output on VCC_OUT_IO.

Use Table 5 **to see which pin is supplied by VCC_OUT_IO and is therefore switchable from +1.8V to +3.3V**

5.2. Reset pin

A low level at SYS_RST# triggers a reset. The module will stay in reset as long as SYS_RST# is grounded. Connect an open drain output or ground switch to SYS_RST#. If unused, leave this pin floating. No external components are required.

NOTICE

SYS_RST# is connected to PMIC_RST_B of the PMIC. Once it is asserted low, PMIC performs cold reset. All voltage regulators are recycled. This also effects output voltage of the SoM.

5.3. Boot Mode

The BOOT_SELx# pins are currently not supported by software. Leaving both pins floating sets the module to default boot medium.

For selecting the boot medium FORCE_RECOVERY# pin is also involved. In case the bootloader is invalid, and the module won't boot any more, this pin can be used to set the CPU into recovery mode.

Table 8: FORCE_RECOVERY# pin settings

FORCE_RECOVERY#	Boot Type
float	foot from fuses
GND	serial downloader

5.3.1. SD/MMC manufacture mode

If no valid boot image is found on the programmed boot devices the SoM switches to SD/MMC manufacture mode before the serial download mode. In the manufacture mode, one-bit bus width is used on uSDHC2 interface to load a boot image from SD card.

It is recommended to have the SDIO_A (uSDHC2) available on the baseboard to boot from SD-card during development

5.3.2. Serial Downloader

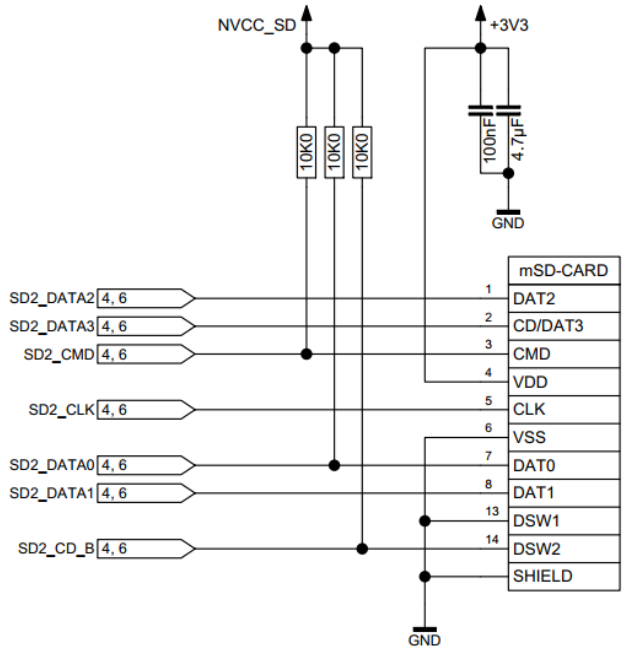
The Serial Downloader provides a means to download a program image to the chip over the USB OTG1 serial connection.

It is recommended to have the OTG1 pins available on the baseboard to recover the SoM in case of a broken image. FORCE_RECOVERY# pin should also be accessible for this purpose.

5.4. SD card

The i.MX8M Mini has three uSDHC interfaces that are compliant to SD/SDIO 3.0 with 200 MHz SDR signalling to support up to 100 MB/sec.

Figure 10: SD-Card connection example



If UHS-I mode is required uSDHC2 should be used as this interface is powered from a dedicated LDO and the supply can be switched from +3.3 V to +1.8 V. This voltage NVCC_SD is accessible on pin B8 to connect external pull-ups.

5.5. Console

The linux console is one of the most important tools to access the SoM. The console can be used to send commands to the SoM and receive information from the SoM.

It is recommended to have the console pins UART_CON available on the baseboard.

6/ Thermal considerations

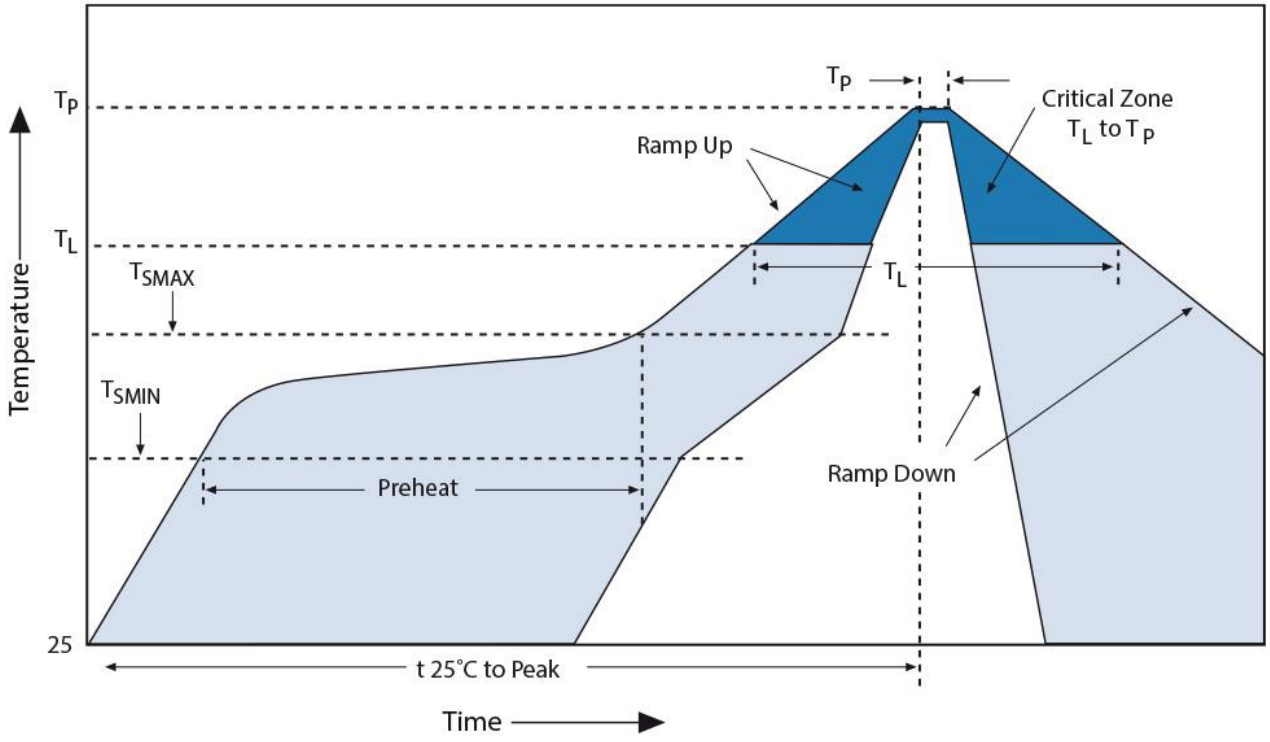
TO BE DEFINED
CONTENT FOLLOWS WITH NEXT DOCUMENT VERSION

7/ Reflow profile

Table 9: Reflow profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (T_{SMAX} to T_P)	3°C/second max.
Preheat Temperature Min (T_{SMIN}) Temperature Max (T_{SMAX}) Time (t_s) from (T_{SMIN} to T_{SMAX})	 150 °C 200 °C 60-120 seconds
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217 °C 60-80 seconds
Peak/Classification Temperature (T_P)	250 °C
Time within 5 °C of actual peak temperature (t_P)	20 seconds
Ramp-down rate	6°C/second max
Time 25 °C to peak temperature	8 minutes max

Figure 11: Reflow Classification Profile



To minimize the stress for the components, it is strongly recommended to solder the SoM during the last reflow cycle of the carrier board manufacturing process.

8/ Technical Support

8.1. First Steps – Startup-Information Baseboard

For the first startup of your Board, which includes the OSM-S iMX8MM SoM, you will find more information about the Software / BSP and additional hardware information at the online documentation.

Please follow the link https://docs.kontron-electronics.de/yocto-ktn/build-ktn-imx/

The online documentation is primarily intended for our Eval-Kit / Evalboard, but will help you also to put your board into operation. Additionally, you will find information how to get access to the Yocto based GitLab software repository and how to make your own software images.

8.2. Extended Support

For detailed technical support please contact:

- E-Mail: support@kontron-electronics.de

8.3. Disclaimer & License Information

The software contained in the device (BSP) contains parts which were licensed as free respectively open source software under the GNU General Public License, version 2 and/or 3, respectively the GNU Lesser General Public License, versions 2.1 and/or 3.0.

You can obtain a copy of the source code of the BSP by following the instructions in the manual at https://docs.kontron-electronics.de/build-system or contact:

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Max-Planck-Str. 6
72636 Frickenhausen
Germany
Web: www.kontron-electronics.de
E-Mail: support@kontron-electronics.de

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